REMARKS

Applicants respectfully traverse and request reconsideration. Applicants would again like to thank the Examiner for allowing claim 40 and for indicating that claims 7–12, 14, and 16–17, would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Objections

The Office Action objects to the Abstract "because it does not provide a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains." Accordingly, an amendment to the Abstract is provided.

On page 2 of the Office Action (reference no. 2) the drawings are objected to because "claim 41's second limitation, wherein the input buffer is operative[ly] to receive the first internal signal from the first internal signal path must be shown or the feature(s) cancelled from the claim(s)." However, Figure 4 illustrates that the input buffer, shown according to one embodiment as the internal I/O circuit 140, is coupled to the first internal signal path shown, according to one embodiment, as AGP bus 190 in order to receive a first internal signal. Further, Figure 5 shows Figure 4 in even more detail according to another embodiment. Accordingly, Figures 4 and 5 show among other limitations in claim 41 "a selector circuit operative to cause the input buffer to provide the first internal signal from the first internal signal path to the first external signal path."

Claim Rejections – 35 U.S.C. § 112

The Office Action rejects claims 41-43 under 35 U.S.C. § 112, first paragraph as failing to comply with the written description requirement. According to the Office Action, "Claim 41's last limitation which states that the selector circuit is operatively coupled to the input buffer to provide the first internal signal from the first internal signal path to the first external signal path is not in the written description." Claim 41 recites:

41. A configurable bus interface circuit comprising:

a first internal circuit operable to provide a first internal signal via a first internal signal path;

an input buffer, operatively coupled to a first external signal path and to the first internal circuit via the first internal signal path, and operative to receive the first internal signal from the first internal signal path and to provide the first external signal on the first external signal path; and

a selector circuit, operatively coupled to the first internal circuit via the first internal signal path, and to the input buffer, and operative to cause the input buffer to provide the first internal signal from the first internal signal path to the first external signal path, and to isolate the first internal signal on the first internal signal path from the first external signal.

As stated above, Figures 4 and 5 provide adequate support for the cited language in claim 41. Further, as stated in the Request for Continued Examination and Preliminary Amendment dated November 19, 2003, support for claims 41, 42 and 43 may be found in the specification at least on page 9, lines 19-30, page 10, lines 1-6, and page 12, lines 5-13 and Figure 4.

Further, Claim 1 as originally filed recites "a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal." Therefore, Claim 1 as originally filed explicitly states that "a selector circuit [is] coupled to the first internal circuit via the first internal signal path, and to the input buffer." Because "the selector circuit [is] operable to select the first internal signal or the first external signal to provide a selected signal", the selector circuit facilitates selection of either the first internal signal or the first external signal. Claim 1 as originally filed also states that the selector circuit is coupled to the input buffer. In other words, the function of the claimed "selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal" is facilitated by "a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer." As a result, the input buffer is operative to receive the first internal signal from the first internal signal path. Since the claims as filed originally are part of the written description, the written description as filed provides adequate support for the claim language in claim 41.

Further, the specification on page 11 lines 19-28 states:

> Alternatively, if the circuit selection logic 185 detects the presence of a graphics controller at the external circuit 150 or detects that any bus bridge signals from the bus bridge 120 onto the AGP bus 190 are intended for the external circuit 150, then the circuit selection logic 185 configures itself to permit the propagation of signals from the external circuit 150 to the AGP bus 190.

As a result, adequate support for the language in claim 41, namely, "an input buffer, operatively coupled to the first external signal path and to the first internal circuit via the first internal signal path, and operative to receive a first internal signal from the first internal signal path and to provide the first external signal on the first external signal path." Consequently, adequate support exists in the claims as filed. Therefore, the objection to both claim 41 and the drawings is improper.

Independent Claim 1:

Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by Lane, et al. (U.S. Patent No. 5,621,900).

Lane

Lane is directed to solving the problem of the differences between the PCI bus standard and previous I/O bus standards which make difficult interfacing peripheral devices designed for the earlier I/O bus standards to the PCI bus. (Col. 1, lines 47-51.) As such, Lane is directed to a computer system that incorporates a PCI or other standard bus with more than one bus of a different standard. (Col. 2, lines 19-21.) Lane teaches resolving a completely different problem from that of the claims. For example, Lane states "The present invention allows the PCI system to have multiple non-PCI buses." (Col. 4, lines 66-67.) Such a configuration would be particularly useful in a mobile computer that has ISA-like buses on the system board and in a docketing station. (Col. 5, lines 1-2.) In contrast, the claims recite "a selector circuit operable to select either the first internal signal or the first external signal" and "an input buffer operable to receive a first external signal via a first external signal path."

The Office Action asserts that:

> Lane discloses a first internal circuit (Figure 1, structure 104) to provide a first internal signal via a first internal signal path (Figure 1, structure 101), an input buffer (Figure 1, structure 113) to [receive] a first external signal via a first external signal path (Figure 1, path between structures 112 and 113), and a

> selector circuit (Figure 1, structure 107) coupled to the first internal circuit [104] via the first internal signal path [101], and to the input buffer [113], the selector circuit [107] operable to select either the first internal signal or the first external signal.

In contrast to the assertion in the Office Action as shown above, the selector circuit, equated to 107 in FIG. 1 of Lane is not coupled to the input buffer (equated to the memory 113). Further, the Office Action fails to show how the selector circuit, equated to host bus bridge 107, is described as operable to select either the first internal signal or the first external signal. Therefore, despite the assertion in the Office Action, Lane fails to describe each and every element as arranged in the claims. Consequently, the Office Action fails to show how Lane anticipates claim 1. As a result, the rejection of claim 1 based on Lane is improper.

Claims 1, 21-23, 25-27, 29-33, and 35-38:

Melo is directed to a computer having a bus interface unit which is coupled between a peripheral bus and a dedicated graphics bus. (Melo Abstract.) The graphics bus can be linked to the bus interface unit by an AGP, while the peripheral bus can be linked to the bus interface unit by a PCI. (Id.) Arbitration for the AGP bus can determine when mastership is granted to an AGP master (i.e., graphics accelerator/controller). (Id.)

Claims 1, 21-23, 25-27, 29-33 and 35-38 are rejected under 35 U.S.C. §102(a) as being anticipated by Melo, et al. ("Melo") (U.S. Patent No. 6,040,845). Claim 1 is rejected entirely based on FIG. 1 of Melo. According to the Office Action:

> Melo discloses a first internal circuit (figure 1, structure 12) operable to provide a first internal signal via a first internal signal path (figure 1, structure CPU bus), an input buffer (figure 1, structure 24) operable to received a first external signal via a first external signal path (figure 1, path between structures 24 and 22), a selector circuit (figure 1, structure 14) coupled to the first internal circuit via the first internal signal path, and the input buffer, the selector circuit operable to select either the first internal signal or the first external signal.

Firstly, the selector circuit equated to northbridge 14 of FIG. 1 is not coupled to the input buffer equated to frame buffer 24. Rather, FIG. 1 shows that northbridge 14 is coupled to the graphics accelerator 20, but is not coupled to frame buffer 24. As such, the Office Action fails to show how Melo describes "a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal." Further, the Office Action

fails to show how Melo teaches "the selector circuit operable to select either the first internal signal or the first external signal." Since the northbridge 14 is not coupled to the frame buffer 24, then the Office Action fails to show how the northbridge 14 is "operable to select either the first internal signal or the first external signal. As such, the Office Action ignores yet another principal limitation in the claims.

Rather than teach coupling the first external signal path to the input buffer, Melo is directed to a completely different problem and does not address the problems sought to overcome by the Applicants.

Further, the Melo reference suffers from the same problems as described in Applicants' "Background of the Invention." Since the northbridge 14 is not coupled to the frame buffer 24, the Office Action fails to show how Melo teaches "a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal."

As to claim 21, Applicants respectfully reassert the relevant remarks made above with respect to claim 1 and again note that this claim requires, among other things, a bus bridge signal from an internal bus bridge and receiving, by an internal circuit, the bus bridge signal and, further, that an internal I/O circuit prevents signals from any external circuit from reaching the internal circuit. Again, as noted above, Melo fails to show "a selector circuit coupled to the first internal circuit via the first internal signal path, and to the input buffer, the selector circuit operable to select either the first internal signal or the first external signal to provide a selected signal." Further, the Office Action only refers to FIG. 1 as a basis for rejecting claim 21. FIG. 1 is merely a block diagram and does not describe any type of function such as "preventing signals from any external circuit from reaching the internal circuit." Additionally, the Office Action fails to show how Figure 1 of Melo, as cited, describes "having an internal circuit," and "receiving a bus bridge signal from an internal bus bridge." Consequently, Melo fails to teach all the elements as arranged in claim 21 namely, "add an internal circuit, receiving a bus bridge signal from an internal bus bridge; and add an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit."

As to claim 22, the Office Action merely relies on FIG. 2 to reject the elements of claim 22. According to the Office Action, the external circuit is equated to the graphics master peripheral target 46 and receives the bus bridge signal from the internal bus bridge, and the

external circuit 46 reflects the bus bridge signal to the internal I/O circuit (equated to structure 40). However, the signals shown in the view of the graphics bus show the transmission of data such as SBA, frame and PIPE with a response AGPGNT messages. The Applicants would like to point out the distinction between bi-directional communication messages such as the transmission of SBA, frame, PIPE and, as a response, receiving an AGPGNT command and "the external circuit reflects the bus bridge signal to the internal I/O circuit." For example, to reflect the bus bridge signal, the actual signal is reflected back whereas no signal reflections are shown in the expansion view of the graphic bus. Further, Applicants respectfully reassert the relevant remarks made above with respect to claims 1 and 21. Additionally, claim 22 includes new and non-obvious subject matter and is also believed to be in condition for allowance. Moreover, the Office Action acknowledges that "Melo's internal circuit does not have [an] input buffer. However, the Office Action fails to show how Melo discloses "receiving a bus bridge signal from the bus bridge . . . without input buffering."

As to claim 23, Applicants respectfully reassert the relevant remarks made above. Further, claim 23 includes new and non-obvious subject matter and is also believed to be in condition for allowance.

As to claims 26, 27, 30, 31, 32, 33, 35, 37 and 38, Applicants respectfully reassert the relevant remarks made above. Further, these claims add new and non-obvious subject matter and are believed to be in condition for allowance.

As to claim 29, Applicants respectfully reassert the relevant remarks made above. The Applicants note that Melo does not teach, among other things, an integrated bus bridge graphics unit coupled to memory that includes an internal circuit operably configured to avoid signals from an external graphics bus. Instead, the Office Action equates the external signal path to the link between frame buffer 24 and display 22 and as such, the northbridge 14 and arbiter 44 do not control the functions of the frame buffer 24 and as such, fail to teach "an integrated bus bridge graphics unit, coupled to the memory bus and further operably coupled to provide a signal to an external graphics bus, the integrated bus bridge graphic unit comprising an internal circuit operably configured to avoid signals from the external graphics bus."

Claim Rejections 35 U.S.C. §103:

Claims 2-5, 13, 15 and 18-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Melo in view of Brickford, et al. (U.S. Patent No. 6,141,021). The Office Action

acknowledges that Melo's disclosure does not explicitly disclose an output buffer and second internal signal path. It is alleged that the Bickford reference discloses an output buffer (structures 170) and provides a second internal circuit via the first external signal path. The Office Action admits that Bickford does not disclose, among other things, a separate second internal signal path for conveying its signal to the output buffer. The Office Action, however, alleges that duplication of working parts of the device which are normally formed in two pieces is well known and that only routine skill in the computer art would be needed to add an additional internal signal path and to integrate the external output path and external input path into one external path. Applicants challenge that such a two-piece system would be needed when such a modification would make the arbiter circuit redundant. Further the Applicants have shown that Bickford teaches away from the claims and one would not be motivated to combine Melo with Bickford.

Consequently, the Office Action fails to establish a prima facie case of obviousness. Applicants repeat the relevant comments above. Bickford also fails to describe the output buffer as operative to receive a second internal signal via the second internal path and to provide the second internal signal via the first external signal path as recited in claim 2. Accordingly, such a combination of the internal circuit, input buffer, output buffer and selector circuit is not taught or suggested by the cited references. Further, as stated above, the references teach against such a combination as claimed. The Applicants hereby incorporate the previous arguments made in all prior Office Action Responses, including those arguments relating to Bickford teaching away from the claims and therefore, the Office Action fails to show motivation for one to combine the references as asserted by the Office Action. As such, the Office Action fails to show how the combination of Melo in view of Bickford establishes a prima facie case of obviousness.

As to claims 3, 4, 5, 13, 15, 18, 19 and 20, Applicants respectfully reassert the relevant remarks made above and again note that these claims add new and non-obvious subject matter. As a result, these claims are believed to be in condition for allowance.

The Office Action acknowledges that Melo does not explicitly disclose multiplexing for the selecting/arbitrating process. Further, the Office Action asserts "hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Mano onto Melo because Mano teaches one the fundamental computer structure in computer design." With regard to the Examiner's assertion of the motivation of one skilled in

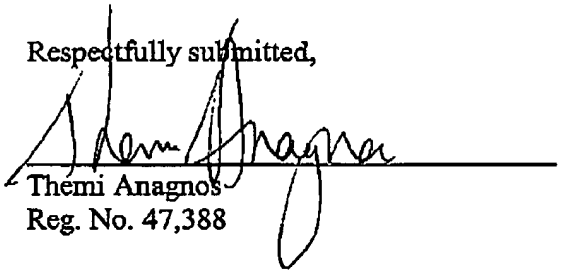
the art to modify the system of Melo with the multiplexing taught by Morris Mano, the Office Action has failed to show how one would be motivated to seek out the teachings of Mano. With regard to claims 6, 28, 39 and 34, Applicants respectfully reassert the relevant remarks made above with respect to the above claims. Further, since the Office Action rejects claims 6, 28 and 39 based on the Applicants' own disclosure, the Office Action improperly uses the Applicants' disclosure as a road map for modifying Melo. As such, the Office Action fails to establish a prima facie case of obviousness for claims 6, 28 and 39. Further, claims 6, 28 and 39 include new and non-obvious subject matter and are believed to be in condition for allowance.

Claim 34 was rejected under 35 U.S.C. §103(a) as being unpatentable over Melo in view of Chen, et al. (U.S. Patent No. 5,850,530). The Office Action acknowledges that Melo does not explicitly disclose an input buffer for receiving the external signal. According to the Office Action, "it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Chen's bridge input buffer onto Melo's bridge because it can reduce the number of retry control signals, which will reduce the number of arbitration attempts." With regard to the Examiner's assertion of the motivation of one skilled in the art to modify the system of Melo in view of Chen, the Office Action fails to show where Melo describes the use of a retry signal and, therefore, one would not be motivated to reduce the number of retry signals through the use of adding the alleged input buffer taught by Chen. As a result, the Office Action fails to establish a prima facie case of prima facie case of obviousness for claim 34.

Accordingly, Applicant respectfully submits that the Claims are in condition for allowance and requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Dated: May 10, 2004

Respectfully submitted,



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